PUBLIC VERSION

COMPETITION COMMISSION OF INDIA

Case No. 16 of 2018

***In Re*:**

Velankani Electronics Private Limited **Informant**

And

Intel Corporation **Opposite Party**

CORAM

Ashok Kumar Gupta
Chairperson

Sangeeta Verma
Member

Bhagwant Singh Bishnoi
Member

Present:

For Velankani Electronics Private Ltd.:	Ms. Smita Singh, Advocate with Ms. Anju Prakash, Legal Head, Mr. Syed Zaid Ahmed, Hardware Design Engineer and Ms. Vinymol Thabi, Hardware Design Engineer at Velankani Electronics Pvt. Ltd.
For Intel Corporation:	Mr. Karan Chandhiok, Ms. Lagna Panda and Mr. Vishnu Suresh, Advocates with Ms. Evangelina Almirantearena, Vice-President and Associate General Counsel Intel Legal Department at Intel Corporation and Ms. Puja Malhotra, SMG, Privacy & Data Security APJ at Intel Technology India Pvt. Ltd.

ORDER UNDER SECTION 26(6) OF THE COMPETITION ACT, 2002

Facts:

1. In the present matter, Information under Section 19(1)(a) of the Competition Act, 2002 (the 'Act') was filed by Velankani Electronics Private Limited ('Informant') against

Intel Corporation ('OP'), alleging, *inter alia*, contravention of the provisions of Section 4(1) read with Section 4(2)(b), 4(2)(c) and 4(2)(e) of the Act.

2. The Informant was stated to be a Bengaluru based private limited company registered under the provisions of the Companies Act, 2013, engaged, *inter alia*, in the business of designing and manufacturing electronic products in India, including 'Servers'. On the other hand, the OP was stated to be a leading multi-national corporation and technology company and one of the world's leading manufacturers of semi-conductor chips. It was stated to be engaged in the designing and manufacturing of a wide range of information technology components, peripherals, computer systems, *etc*. and in manufacturing and distribution of electronic devices relating to communication and computing such as processors, chipsets, motherboard/server-board, integrated circuit, network interface controllers, flash memory, *etc*.

3. The Informant, in the Information filed, submitted that a 'Server' is a type of computer different from other types of computers such as laptop, desktop, tablet *etc*. The Server has various sub-assemblies such as processor, server-board, chassis, memory disk *etc*. Presently, the Informant simply assembled a Server by putting together various sub-assemblies and sold the Server in the market. For the said purpose, it had executed a Manufacturing Enablement and Licensing Agreement ('MELA') with the OP. However, in order to design its own Server, it sought to manufacture its own server-board so as to have a competitive edge. Purchasing the server-board from competitors to fit into the Informant's Server would unduly inflate the cost of the Informant's final Server. Hence, the Informant sought to manufacture its own server-board.

4. It was stated that for a Server to work, its various sub-assemblies need to interface with each other. One such most important sub-assembly is the 'processor'. A processor cannot be interchanged with any other product nor be manufactured by the Informant itself as it is not easily reproducible at a reasonable cost in the short-term. As per the Informant, the OP is the dominant player in the market for processors globally as well as in India. Thus, to make a workable Server, the server-board proposed to be manufactured by the Informant needed to interface with the processor manufactured by the OP. As such, for manufacturing such a compatible server-board, the Informant required access to the reference design files and simulation files of server-boards from

the OP so as to incorporate the same in the design of its server-board. The OP's design files were hence, stated to be very essential for the Informant. In the absence of such files from the OP, the Informant could not develop its server-board which would interface with the processor of the OP.

5. The Informant alleged that the OP precluded the Informant from designing/manufacturing its own server-boards, by refusing to provide it complete reference design files and simulation files, like the OP provided to other Original Equipment Manufacturers ('OEMs') such as Dell, HP, Lenovo *etc*., despite the Informant's numerous requests in this regard since July 2017. It was alleged that without the same, the Informant could not manufacture server-boards compatible with the processor of the OP. Such conduct of the OP was alleged to amount to abuse of dominant position as it (i) led to denial of market access to the Informant in violation of the provisions of Section 4(2)(c) of the Act; (ii) restricted the production of Servers and market therefor and also limited technical/scientific development relating to Servers in violation of the provisions of Section 4(2)(b) of the Act; and (iii) amounted to abuse of dominant position in the market for processors for Servers to protect the market of Servers in violation of the provisions of Section 4(2)(e) of the Act.

6. The Commission, after considering the matter, held a preliminary conference with the parties on 12.07.2018 wherein detailed arguments from both sides were heard. Before the conference, the OP also filed a detailed reply to the Information. Post the conference, detailed written submissions from both parties were also received along with undertakings to the effect whether reference design files and simulation files were provided by the OP to the Informant or not.

7. Based on the facts and material available on record, the Commission, *vide* order dated 09.11.2018 passed under Section 26(1) of the Act, opined that there existed a *prima facie* case of contravention of the provisions of Section 4 of the Act by the OP in the matter, as detailed therein.

8. Accordingly, the Commission directed the DG to cause an investigation to be made into the matter and submit an investigation report.

Investigation by the DG:

9. To investigate the matter, the DG issued notices to the Informant, the OP and various third parties like Dell, Acer, HP, AMD, TCS, IBM, Cognizant, HCL, Wipro, Infosys, Lenovo, *etc*. to furnish certain information and documents. Further, the DG analysed the background of the industry including how a server is different from other types of computers, the various components of a server, how a 'processor for server' is different from processors for other types of computers, the historical background and evolution of development of a processor/micro-processor by the OP and categories of latest processors of the OP such as Intel Core, Pentium, Celeron, Atom, embedded and Xeon, meaning of various technical terms/working of components, server market in India *etc*.

10. The DG then identified the following issues for investigation and gave its findings on the same as follows:

(i) What is the relevant market(s) in terms of Section 2(r) of the Act?

The DG distinguished micro-processors from other components of computers as well as micro-processors across end-products. Further, the DG analysed the dependency of server-board manufacturers on the provision of reference design files and simulation models from the micro-processor manufacturer. As such, since the allegations in the present matter pertained to the denial of files by the micro-processor manufacturer, the relevant market was identified by the DG as the market for 'Processors for Servers in India'.

(ii) Whether the OP holds a dominant position in the delineated relevant market(s)?

The DG analysed various factors stated under Section 19(4) of the Act, including market share, size, resources and economic power, size and importance of competitors, economic power of the OP including advantages over competitors, dependence of consumers, entry barriers and market structure. The DG, on the basis of analysis of the same, observed that the OP was able to operate independently of the competitive forces in the delineated relevant market and that its position of strength affected its competitors, consumers and the relevant market in its favour. Hence, the DG found the OP to be the dominant player in the identified relevant market.

(iii)Whether the OP has abused its dominant position in the relevant market?

To examine this aspect, the DG formulated the following three issues: -

a) Whether the conduct of the OP as alleged by the Informant amounts to abuse of dominant position by denial of market access, in contravention of the provisions of 4(2)(c) of the Act? and

b) Whether the OP, through its alleged conduct, limited and restricted the production of servers and market therefor as well as limited technical/scientific development relating to servers in the market in contravention of the provisions of Section 4(2)(b) of the Act.

The DG, upon analysis of the submissions made by the Informant and the OP, concluded with respect to reference design files that there was no denial of access to any file by the OP as complete files for Buchanan Pass and Wolf Pass on Purley Platform were provided to the Informant *via* Intel Business Link ('IBL') (now renamed as Resource Data Centre 'RDC') and no files for Sawtooth Pass and Silver Pass ever existed.

With respect to simulation models, the DG, from the submissions of the OP and third-parties, observed that Hewlett Simulation Program with Integrated Circuit Emphasis ('HSPICE') and Input/Output Buffer Information Specification ('IBIS') are both complete simulation models using which server-boards can be developed. The DG, upon analysis of the Informant's e-mails and submissions made by the Informant's simulation service provider, concluded that complete set of HSPICE files was provided by the OP to the Informant and the same were sufficient for the Informant to develop its server-boards as per the opinion of the Informant's own experts.

Further, the DG noted that the Informant was given access to the important resources prepared by Intel for designing a server-board, *i.e.* [redacted] and [redacted]. The [redacted] is [redacted], while [redacted]

[redacted].

Hence, the DG concluded that there was no denial of market access to the Informant on the part of the OP in contravention of the provisions of Section 4(2)(c) of the Act and there was no limitation and restriction on the production of Servers and market therefor or limitation of technical/scientific development relating to servers by the OP in contravention of the provisions of Section 4(2)(b) of the Act.

c) Whether the conduct of the OP as alleged by the Informant amounts to abuse of dominant position in the market for 'Processor for Servers' to enter into or protect market for 'Servers' in contravention of Section 4(2)(e) of the Act.

The DG noted that the OP's market share in the 'market for servers' was below [redacted] from the year 2016 to 2019. Further, the DG did not find any evidence suggesting that the OP denied any access to the information which was required by the Informant to enter into the server market as an OEM. Thus, the DG did not find any contravention of the provisions of Section 4(2)(e) of the Act also.

Proceedings before the Commission:

11. Upon consideration of the investigation report submitted by the DG in its ordinary meeting held on 15.09.2021, the Commission forwarded an electronic copy of the same to the parties, giving them an opportunity to file suggestions/objections, if any, thereto and appear for an oral hearing through video conferencing mode.

12. Suggestions/objections to the DG Report were filed by the OP agreeing with the finding of the DG that it has not contravened any provisions of the Act. However, it disagreed with the findings of the DG regarding delineation of relevant market and its dominance therein. Nonetheless, it stated that it is not objecting to the findings of the DG on these issues as such issues no longer remain relevant for adjudication of the present matter and accordingly, may be left open.

13. On the other hand, on behalf of the Informant, no suggestions/objections to the DG Report were filed. Rather, it was stated that during the pendency of the investigation, the OP has provided to it access to the requisite files for designing server-boards/servers compatible with the OP's latest processor [redacted] in 2020. Further, it was stated that the OP has also streamlined its access portal to make access easy/convenient and the Informant is hopeful that the OP shall continue to provide non-discriminatory access to the Informant and all other designers and manufacturers of server-boards/servers in India. As such, since the Informant's grievance about denial of essential information by the OP stands satisfied, it stated that its complaint on account of denial of access has become infructuous. Hence, though the Informant did not accept the conclusions drawn by the DG in its report that there was no abuse of dominant position by the OP, it decided not to press its case against the OP any further.

14. On 11.11.2021, the Commission heard the parties through Video Conferencing and decided to pass an appropriate order in the matter.

Analysis and Findings:

15. The Commission has perused the Information, the investigation report submitted by the DG, the submissions filed by the parties and also heard the oral arguments addressed by the respective learned counsel(s) for the parties.

16. The Commission notes that the grievance of the Informant in the present matter seems to be denial of access to complete reference design and simulation files by the OP to the Informant, which may enable the Informant to design and manufacture its own server-boards compatible with the micro-processor designed and manufactured by the OP. The Informant's allegation was that, since the OP is the dominant player in the micro-processor for server market, the server-board developed by the Informant needs to interface with the micro-processor of the OP so that both such sub-assemblies can fit into and be part of one marketable server. It was alleged that denial to the Informant is being made by the OP in a discriminatory manner, as access to such files is provided by the OP to other OEMs such as Dell, HP, Lenovo, *etc*. Hence, since the OP is the dominant player in the micro-processor for the server market, its denial amounts to

abuse of dominant position by it in contravention of the provisions of Section 4 of the Act.

17. Before proceeding to make further analysis, the Commission adverts to the submission made by the OP that, in the present matter, since the DG Report has not found any abuse on part of the OP, delineation of a relevant market and ascertaining the position of dominance of the OP therein becomes irrelevant. As such, these issues may be left open by the Commission and finding on the same may not be given.

18. In this regard, the Commission notes that the DG, after carrying out comprehensive investigation, has given a finding on the dominance of the OP and of no contravention by it relating to the alleged conduct; the same pre-supposes the existence of a concrete definition of a relevant market as well. Therefore, for the Commission also, in order to give a definitive finding/conclusion on the conduct of the OP, it becomes imperative to deal with such issues rather than leaving them open.

19. In view of the above, the Commission is not inclined to accept the submission made by the OP and the Commission proceeds to examine and analyse the conduct of the OP.

Relevant Market

20. The grievance of the Informant is the alleged denial of access by the OP to all files/documents/information necessary for enabling the Informant to design/develop and manufacture its own Server-Boards which are compatible with the Micro-Processors manufactured by the OP, in a discriminatory manner.

21. In order to assess the conduct of the OP under the provisions of Section 4 of the Act, a relevant market needs to be delineated first. If the OP is found to be in a dominant position in such relevant market, the Commission is required to analyse its alleged abusive conduct.

22. For the purposes of defining the relevant market, the Commission shall delineate both the 'relevant product market' in terms of Section 2(t) read with Section 19(7) of the Act, and the 'relevant geographic market' in terms of Section 2(s) read with Section 19(6) of the Act.

23. With respect to the 'relevant product market', it is noted from the investigation report that micro-processors are a distinct product in themselves and not substitutable with any other component of a computer. Further, it is also noted that micro-processors across end-products are also not substitutable, as the same have different technical characteristics and capabilities such as processing power, computing power, consumption, memory accessibility, *etc*.

24. Based on the submissions made by the parties before the DG, it is gathered that the development of a server-board is dependent on the architecture of the micro-processor. A micro-processor is responsible for carrying out all mathematical and logical operations and computing of a device/system. In order to execute the operations, a micro-processor interacts with communication channels known as 'buses', which connect the micro-processor with other components in a computer to input programming instructions and data to the micro-processor and output data from the micro-processor. This underlines the requirement of the simulation models and basic reference designs, which gives the first starting point for server-board designers who are ignorant about the internal design of the micro-processor or other components, and such reference design and simulation models facilitate how to develop the interaction of a micro-processor or other parts in a server-board (such as memory card, chipsets, *etc*.) with each other.

25. The DG has noted that as per the report of the Economic Expert submitted by the Informant, there is a vertical economic relationship between the OP and the Informant. This arrangement is due to the nature of the industry, where the micro-processor is the intermediary product to be used in the server-board designing. Though the OP has, before the DG, submitted that the relevant product market ought to be the market for 'Server' or the market for 'server-boards', it has been accepted both by the OP and the Informant that the simulation models are a must for server-board designers and it can only be sourced from the manufacturer of the micro-processor. This itself lays the dependency of the server-board designers, including that of the Informant, on the OP for necessary simulation models and details required.

26. Considering the Information and the averments made therein, the Commission notes that even though the denial of files by the OP to the Informant is stated to restrict/impede the entry of the Informant in the 'Server' or 'server-board' market, the conduct complained of is with regard to the design files which enables the Informant to design a product compatible with the OP's processor. It is the purported denial of access to such files which has been alleged to be abusive by the Informant.

27. As such, the relevant product market in the present matter is '*the market for Processors for Servers'*.

28. With regard to the 'relevant geographic market', it is noted that the market conditions for micro-processors for Servers across India are homogeneous. As such, the relevant geographic market is '*India*'.

29. Accordingly, the relevant market in the present matter is delineated as the market for "*Processors for Servers in India"*.

Dominant Position

30. The Commission now proceeds to assess the position of dominance of the OP on the basis of factors stated under Section 19(4) of the Act, in the delineated relevant market.

31. The market share data in the DG Report shows that the OP has strength over other players in the processor for server segment. The distribution figures of micro-processors as well the revenue figures of the OP from sale of its products in India, as brought out in the DG Report, indicate that the OP has substantially large resources as compared to its competitors. Multiple government tenders also reflect that the OP's processors are mentioned as eligibility conditions. The entry barriers into the market in terms of R&D cost and technology have also been considered. Thus, it is observed that the OP is able to operate independently of the competitive forces in the delineated relevant market and its position of strength affects its competitors, consumers and the relevant market in its favour. Further, it is noted that the Commission, in its previous decision in *ESYS Information Technologies Pvt. Ltd. v. Intel Corporation and Others, Case No. 48 of 2011 decided on 16.01.2014*, had concluded that the OP is dominant in the market of Micro-Processors for Servers in India. No change in the market structure since then has been brought to the attention of the Commission by the OP.

32. Hence, the Commission holds the OP to be in a dominant position in the relevant market of *"Processor for Servers in India"*.

Abuse

33. Once the relevant market has been delineated and the position of dominance of the OP therein is established, the Commission now moves to assess the abuse of dominant position, if any, by the OP.

34. At the outset, the Commission notes that the DG, in its investigation report, has found no abuse of dominant position by the OP. In this connection, the Commission notes that though the Informant has stated that it disagrees with such conclusion of the DG, it has not filed any suggestions/objections in rebuttal thereto and has also not made any oral submissions in this regard, except stating that it does not agree with the conclusions drawn by the DG. The only submission which the Informant has made is that since during the course of the investigation, it has been provided access to the relevant files by the OP, it does not seek to pursue the matter further.

35. Considering the above, based on the investigation report submitted by the DG and material on record, the Commission proceeds to analyse the alleged abuse on the part of the OP, if any.

36. With regard to the reference design files, there is no dispute that under the Purley Platform, the OP had released four products/passes *i.e.* Buchanan Pass, Wolf Pass, Silver and Sawtooth Pass. In the Commission's *prima facie* order as well as in the DG Report, it has been consistently found that, for such Purley Platform products, the OP had uploaded on the IBL/RDC, the reference design files for Buchanan Pass and Wolf Pass to which the Informant had access. For Sawtooth Pass and Silver Pass, no reference design files were developed by the OP so there was no possibility of uploading the same and the Informant could not have been provided access to the same. Thus, there is no question of any denial to the Informant of any reference designs.

37. As far as simulation files are concerned, it is noted that the Informant had listed the following files/information, of which it required the latest/updated versions, to integrate the OP's processors with its servers/ server-boards:

1	[redacted]
2	[redacted]
2.1	[redacted]
2.2	[redacted]
2.3	[redacted]
2.4	[redacted]
2.5	[redacted]
2.6	[redacted]
2.7	[redacted]
2.8	Simulation models for complete processor(IBIS,SPICE)
2.9	[redacted]
3	[redacted]
4	[redacted]
5	[redacted]
6	[redacted]
7	Purley Collateral list document access-list attached (3 pages)

38. As per the Informant, files/information requested *vide* Sl. Nos. 1 to 6 of the above list were standard information required for integration. This includes file/information required at Sl. No. 2.8 which relates to Simulation Models for complete processor (IBIS, SPICE). At Point 7, a 'Purley Collateral List' is mentioned which itself contained a list of 700 files which was provided in an excel sheet to the Informant by the OP. The Informant had submitted that, out of these 700 files, it could not access 82 files on the RDC. Further, these 700 files did not contain the IBIS simulation files requested by the Informant. As per the Informant, the SPICE simulation files provided to it did not perform the required function (*namely* simulation for server-board) fully and accurately. Further, simulation models were not provided for [redacted] and [redacted] ([redacted]). As per the Informant, in order to design server-boards and integrate/interface the same with the OP's processor, in addition to its in-house team of engineers, the Informant had taken assistance from industry experts [redacted] and [redacted], and the said experts have also maintained that, in order to interface the OP's processor with the server-board being designed, it was critical to have IBIS files, and that the SPICE files made available were not capable of performing the desired simulation function.

39. When asked by the DG to offer comments in this regard, the OP submitted the status of these 82 files in the following terms:

SI. No.	Category	No. of files
1.	Downloaded by the Informant	25
2.	Accessible to the Informant	13
3.	Internal files of the OP	11
4.	Expired due to Obsolescence	33
5.	**Total**	**82**

40. The allegations of the Informant pertain to non-accessibility to the full collateral of 700 documents along with reference design files for all the four passes as well as the IBIS format of simulation model. The Informant, on Affidavit dated 04.08.2018, had submitted before the Commission that it did not have access to 82 files out of 700. In this regard, the OP had submitted that the Informant had already downloaded 25 files out of 82 before submitting the Affidavit. The OP, in this regard, also submitted the list of these 25 files downloaded by the Informant with date and time of each downloaded file. Further, the OP submitted that out of the remaining 57 files, the Informant had access to 13 files, 11 were internal files and balance 33 files have become obsolete. On the issue of obsolescence, the OP submitted that certain files uploaded on RDC expire as and when they become redundant or when they are revised and replaced by new files, and thus, are not of utility anymore in the designing server-boards based on current Intel platform.

41. For acquiring further information on the status of these 44 files (11+33), both the OP and the Informant were asked by the DG to provide details. The Informant submitted that, out of the 82 files, it now has access to 34 files and the remaining 48 files are still inaccessible. The Informant further submitted that these 48 files also included [redacted]'), which were required for designing a server-board. On the other hand, the OP provided the list of these remaining 44 files explaining the nature of each file.

42. Upon analysis of the submissions of both the Informant and the OP in this regard, the DG observed that many documents in the Purley collateral list were updated with a different file number and the replaced file was either downloaded by the Informant or accessible to the Informant. Further, the DG noted that there was obscurity in the

submissions of both the Informant and the OP with respect to the files not being accessible. Whereas the Informant listed 48 files as being not accessible, the OP affirmed that the Informant did not have access to only 22 files out of 82 documents (after considering accessibility to replaced files). The DG checked such obscurity and noted that the Informant lists file number #[redacted] as inaccessible, but the OP placed on record evidence that this particular file was in fact mailed to the Informant on 08.02.2018 itself. The DG further observed that the same is also reflected in the matter of other files where the OP's server records shows that the Informant has downloaded the updated version, but the Informant has submitted that it does not have access to these files.

43. Further, regarding accessibility of the RDC, the DG also inquired from certain third-parties. Amongst such third-parties, few had Service Level Arrangement ('SLA') with the OP. It was found by the DG that documents like [redacted], issued to announce release of any upcoming information or model, were no longer functional, as they had served their purpose with the release of the model/information by the OP on RDC. Further, it was gathered from third-parties and publicly available sources that proprietary information of the OP, *i.e.* designs of all the four passes, *viz.* Buchanan Pass, Wolf Pass, Sawtooth Pass and Silver Pass, were not required for ensuring the interoperability function in the designing of servers. Only reference designs were required which were provided by the OP to the Informant.

44. As per the OP, the most important resources prepared by it for designing a server-board are the [redacted] and the [redacted]. The Purley [redacted] is a [redacted], while the [redacted]. As per the OP, both Purley [redacted] and [redacted] documents can be downloaded free-of-charge from its RDC and the same have been provided to the Informant which are sufficient for the Informant to design its server-boards. The OP even submitted that in case of a deviation from the Purley [redacted], it had offered the Informant a solution: it

had agreed to review the details of such deviations and help the Informant simulate the deviating aspects of the design. However, the Informant never provided any such design files to the OP for review and never requested any such support.

45. In view of the above, the DG noted that there was no denial of access to the Informant as the files of Purley collateral list were accessible to the Informant and the updated version(s) were made available to the Informant, if certain document(s) became obsolete.

46. Next, the DG examined certain other issues, *inter alia*, relating to whether (i) HSPICE format was an alternative to IBIS format of simulation models; (ii) IBIS models were provided by the OP to the Informant; and (iii) complete set of HSPICE files was provided by the OP to the Informant and the same were sufficient for the Informant to develop its server-boards.

47. In this regard, the DG first examined the concept of simulation and observed that computer simulation is the process of mathematical modelling, performed on a computer, which is designed to predict the behaviour of or the outcome of a real-world or physical system. Since simulation allows to check the reliability of chosen mathematical models, computer simulations have become a useful tool for mathematical modelling of many natural systems. The DG then explained the term Signal Integrity ('SI') that SI addresses two concerns in the electrical design aspects – the timing and the quality of the signal. The goal of SI analysis is to ensure reliable high-speed data transmission. Advances in high-performance sub-micron micro-processors, the arrival of gigabit networks and the need for broadband Internet access necessitates the development of high-performance packaging structures for reliable high-speed data transmission inside every electronics system. SI is one of the most important factors to be considered when designing such packages and integrating these packages.

48. The DG further noted that simulation of a system is represented as the running of the systems model. There are different formats of simulation files such as SPICE format, HSPICE format, IBIS format and [redacted]. As regards comparison between SPICE and IBIS Models, the DG observed that IBIS models are behavioural models, and therefore,

allow faster simulation runs than SPICE. A speed factor of 25 times is not uncommon. But this lead is getting shorter with optimised algorithms in SPICE and is of less concern with faster workstations. Behavioural models do not reveal any proprietary transistor structures. Non-Disclosure Agreements ('NDAs') are no longer needed. Another very important advantage is the compatibility of IBIS with almost all signal integrity tool vendors. IBIS models do not have special proprietary simulation levels as opposed to SPICE. However, IBIS lacks information about internal wiring. This makes buffer behaviour less understandable for the user and diminishes possibilities to influence buffer characteristics for a targeted system environment.

49. The DG also looked into various technical aspects of simulation models in expert publications *e.g.* a paper published by ResearchGate under DesignCon 2016 titled "*Measurement and Simulation of a High-Speed Electro/Optical Channel*", the website xilinx.com, the words of industry expert Bonnie Baker and the book *Semiconductor Modelling* authored by Roy G. Leventhal and Lynne Green. From the above, the DG opined that industry experts prefer IBIS model on the ground of speed, but SPICE models are considered more accurate. The DG noted that this opinion of expert is in consonance with the submission of the OP which stated '*IBIS programs are not suitable for high-speed simulation above 1 gigabytes per second*'. The above reports also suggest that where semi-conductor manufacturer companies rely on SPICE model of simulation, engineers prefer IBIS due to time factor.

50. The DG thereafter also obtained views in this regard from the competitors of the OP in the relevant market *i.e.* AMD and IBM. Both denied releasing simulation models in the IBIS format. They stated that both IBIS and SPICE models are industry standards. The DG also approached other third-parties who are server-board designers like CISCO, HP, L&T, WIPRO, ZOHO *etc.* and noted that they gave divergent views regarding necessity of IBIS model of simulation.

51. From the submission of the Informant, the DG noted that, to design a server-board, the Informant had approached the following two major Simulation Service Providers: (i) [redacted]; and (ii) [redacted]. When the DG inquired from both about the requirement of IBIS simulation files, the submission of [redacted] was different from that of the Informant, who had stated that both the experts insisted on

IBIS format of simulation models. [redacted] stated that it was able to run SI test using SPICE models. To check the veracity of such submission of [redacted], the DG analysed the correspondences between the Informant and [redacted].

52. The DG noted that though [redacted], in its e-mail dated 18.01.2018, had asked the Informant to get IBIS files from the OP, it had also, in another e-mail, stated that to meet the challenges surrounding simulation, the best way is to follow the guidelines provided in [redacted] as, any deviations can be shared with the OP because the OP had agreed to lend support on telephonic call on 01.03.2018.

53. As far as [redacted] is concerned, the DG noted that the e-mail dated 13.07.2018 sent by [redacted] to the Informant stated that it does not have resources to correct/generate SPICE files.

54. The DG also identified an e-mail dated 22.02.2018, wherein it was recorded by the Informant that for SI, the OP had recommended to follow the [redacted], and if not followed, the Informant needed to share the design files with the OP for SI assistance. Further, an e-mail dated 01.03.2018 also recorded the fact that the OP was assisting the Informant in SI of its server-board along with [redacted]. On review of the e-mails exchanged between the OP, the Informant and [redacted], the DG observed that, till 13.03.2018, all of them were regularly interacting with each other to resolve the issues faced in simulation test using HSPICE models.

55. The DG noted that as per the OP's internal assessment, SPICE models were working to the satisfaction of the OP's team. This was evidenced from an e-mail dated 13.07.2018 whereby the OP team internally communicated to their management that *'But the models worked perfectly well as expected... Please note that HSPICE models were unencrypted and ideally can be used by any SI tool without any modifications.'* The OP's employees also mentioned that they could not find the IBIS model for CPU but HSPICE models available for CPU interface and the same were referred to the Informant.

56. In this regard, the DG questioned the OP regarding the allegation of denial of access of IBIS simulation files to the Informant in a discriminatory manner. The OP submitted that it developed only [redacted] simulation models for Purley Platform in IBIS format: [redacted]

[redacted]. As per the OP, all these were available on RDC and were downloaded by the Informant. The Informant also admitted that these [redacted] simulation models were made available to it under the Purley Platform. However, the Informant submitted that such files were not significant from the Informant's design perspective.

57. The DG, based on analysis of different simulation models, the reports of industry experts, replies of third-parties as well as submissions of the Informant and the OP, hence, concluded as follows:

(a) HSPICE format was an alternative to IBIS format of simulation models. The only requirement was that given model should be complete in all respects. The OP, as per prevalent industry practices, was under no compulsion to create simulation models in the IBIS format.

(b) The IBIS models developed by the OP for the Purley Platform were in fact provided by the OP to the Informant.

58. Regarding the Informant's allegation that the OP did not provide it the complete set of HSPICE simulation model, the DG observed from the communication dated 18.04.2018 between [redacted] and the Informant that [redacted] did communicate to the Informant that *"All the information you need is contained the supplied files. You just need to understand the SPICE syntax well enough to find out what the SPICE file defines for stimulus, netlist, and results."* Hence, as per the DG, the same communication confirmed the completeness of the files of SPICE model for necessary simulation.

59. Further, the Informant had also alleged that simulation models of [redacted] and [redacted] ([redacted]) ([redacted]) were also denied by the OP. However, the DG, on review of the list provided by the OP of the simulation models provided by it to the Informant, noted that in respect of [redacted], the simulation files were in fact accessible to the Informant and were also downloaded by Informant. Further, in respect to [redacted] ([redacted]), the DG, from the submission of the OP, noted that the OP did not develop any simulation model as

the standards were strictly followed. Rather, the OP provided a '[redacted]' for [redacted], which allowed a server-board designer to do the required testing for verification of the interface. Thus, the DG did not find any merit in the allegations of the Informant in this regard as well.

60. Another allegation levelled by the Informant was that one particular file, #[redacted] (being an essential file), was not made accessible to it by the OP. In this regard, the DG, firstly, from the analysis of the e-mail correspondences between the Informant and the OP, noted that, as the Informant initially did not provide the specific file number it was seeking, there arose some confusion in the matter. The DG observed that RDC contains vast resource data, hence, reference to the specific file number is the best way to locate a file instead of the subject-matter of the file, which might have possibilities of a message displaying either denial or non-availability of files. Thereafter, in its e-mail dated 31.01.2018, the Informant provided the wrong file number, #[redacted], instead of #[redacted], which it continued to mention wrongly even in subsequent e-mails.

61. In this regard, the OP submitted before the DG that such file which was contested by the Informant as 'essential' to its designing process was released on a 'pilot basis'. This information was shared by the OP in a presentation which was downloaded by the Informant as evidenced from an e-mail dated 08.02.2018. The OP submitted that as [redacted] was on a 'pilot basis', it was not made part of 'collaterals' released on Purley Platform. After analysing the evidence on record, the DG noted that [redacted] file was not an 'essential' file required for simulation. The file was also not part of released Purley Collateral List by the OP. Further, the Informant was privy to the information released as 'collateral' by the OP on its RDC portal and nowhere did such file (which was on pilot basis) prove to be an impediment to the Informant's efforts for server-board designing.

62. On the basis of above detailed analysis, the DG came to the conclusion that the Informant had access to the collaterals of the Purley Platform and downloaded most of them. The OP was not restricting access of the Informant to such collaterals in a discriminatory manner, as alleged. Further, certain internal files were also shared by the OP with the Informant on its request. The e-mail correspondences between the OP and

the Informant indicated overlapping references to RDC access and MELA arrangement and confusion arose from the same. It was seen that the Informant was not only requesting reference design files of [redacted] ('[redacted]') – which in common parlance refers the 'design' which is created by the manufacturer of processor as reference or guide to the server board designers which can be used by them to check any deviation to their own designs, of Purley platform but also requested for reference design files of commercial products developed by the OP under the Purley Platform. Even the files which were covered under deliverables of MELA contract were asked by the Informant in its request for design files from the OP.

63. With respect to the Informant's submission that the IBIS model of simulation model is necessary, the DG found that both IBIS and HSPICE act as an acceptable standard for simulation model. While users (server board designers) prefer IBIS for their ability to make fast simulation, many semi-conductor manufacturers do not use the IBIS model for their inherent limitation of being inaccurate beyond a speed level. The OP did not release complete simulation model in IBIS format, rather it created the same in HSPICE, a few in IBIS, along with its proprietary format [redacted]. Even other processor manufacturers such as IBM and AMD stated that they do not prepare simulation models in IBIS format. Based on analysis of different simulation models, reports of industry experts, replies of third-parties as well as arguments of the Informant and the OP, the DG found that both HSPICE and IBIS are accepted as standards by the industry. The evidence furnished by the OP showed that it provided to the Informant, simulation models it had generated in IBIS as reference collaterals. The OP had released [redacted] IBIS files as part of Purley collateral list of 700 documents, and the Informant also accepted that these files were accessible and downloaded by it. Hence, the Informant's allegation that the OP deliberately withheld reference files or simulation models in IBIS format, restricting access to files in violation of Section 4(2)(b), was not found to be correct by the DG. With respect to an [redacted] file #[redacted], which was not part of Purley collateral list of 700 documents, evidence has come forth which indicated the experimental nature of the document. The OP said that it released this file on a pilot basis and it was proved that the Informant was privy to this information. Hence, the 'essentiality' of such file as claimed by the Informant, was proven incorrect. With

respect to the Informant's allegation that OP did not provide any simulation models for [redacted] and [redacted] ([redacted]), the DG found that the simulation models for [redacted] were accessible to the Informant and it had downloaded them. Regarding simulation model for [redacted], the DG found that the OP did not develop any simulation model as the industry standards are followed and no separate simulation model is required for same. The OP only provided '[redacted]' for [redacted] on IBL which was accessible to the Informant.

64. In view of the above analysis, the DG concluded that the Informant was given access to the [redacted] and '[redacted]', *i.e.* [redacted] of Purley Platform along with simulation models and other collaterals of Purley Platform by the OP. As such, there was no denial of market access by the OP to the Informant, in contravention of the provisions of Section 4(2)(c) of the Act.

65. Further, the DG found that access to RDC portal enabled around [redacted] Indian entities/ parties to develop their technologies. It was noted that Indian entities like L&T and Infosys were engaged in server-board designing on behalf of other OEMs. It was also noted that the OP had also entered into MELA with the Informant in India, which indicated contrary to any intention to block its access to the server market. As such, the DG found that there was no limiting or restricting production of Servers and market therefor by the OP and also no limiting technical/scientific development relating to Servers in the market by the OP, in contravention of the provisions of Section 4(2)(b) of the Act.

66. The DG lastly noted that Section 4(2)(e) of the Act envisages presence of two relevant markets, one in which the enterprise should be dominant and the other which the enterprise seeks to enter into or protect. In the present case, the Informant had specified the second relevant market as the 'Market for Servers', which had been contested by the OP as the only relevant market in the case. The Informant had alleged that the OP is using its dominance in the market for 'Processor for Servers' to enter or protect its position in the 'Market for Servers'.

67. The OP stated before the DG that it has a presence in the 'Market for Servers' but the same was below [redacted] from the year 2016 to 2019. After analysis of the submissions of both the Informant and the OP along with third parties, the DG observed that the OP did not engage in alleged refusal to provide essential information to the Informant; instead, access to the information *via* RDC portal had enabled the OP's competitors in the server market to grow. Since there is no evidence to suggest that the OP had denied access to the information which was required by the Informant to enter into the server market as an OEM, the DG concluded that the allegation of leveraging does not hold against the OP. Hence, contravention of the provisions of Section 4(2)(e) of the Act by the OP was also not proved.

68. In view of the foregoing, the Commission is of the opinion that there was no deliberate denial of any requisite file (reference design file or simulation file) by the OP to the Informant. Reference design files which existed only for Buchanan Pass and Wolf Pass and not for Sawtooth Pass and Silver Pass, had been provided by the OP to the Informant. Further, HSPICE simulation model and IBIS simulation format were found by the DG to be substitutable with each other and evidently, complete set of SPICE simulation model and IBIS files (as existed on Purley Platform) had been made available by the OP to the Informant. The SPICE files provided seem to be sufficient for the Informant to develop its own server-boards.

69. Resultantly, as the OP is not found to have denied access to the Informant to any requisite reference design files and/or simulation files, no abuse of dominant position can be attributed to the OP.

Conclusion:

70. In view of the above, the Commission is of the opinion that no case of contravention of the provisions of Section 4 of the Act by the OP is made out in the present matter. As such, the matter is directed to be closed forthwith in terms of Section 26(6) of the Act.

71. The Commission directs that two versions of the present order may be prepared, *i.e.*, a non-confidential *qua* parties version and the public version. The same shall be prepared keeping in mind the confidentiality requests made by the parties, the orders passed in this regard and the provisions of Section 57 of the Act.

72. The Secretary is directed to inform the parties, accordingly.

Sd/-
(Ashok Kumar Gupta)
Chairperson

Sd/-
(Sangeeta Verma)
Member

Sd/-
(Bhagwant Singh Bishnoi)
Member

New Delhi
Date: 03.12.2021